REMARKS

Claims 1-5 and 7-12 are presented for examination.

Claims 8, 10 and 12 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

In response, these claims have been amended to address the issues raised by the Examiner.

Claims 1-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Yamamura and Rosenthal et al.

This rejection is respectfully traversed for the following reasons.

Claim 1 recites an apparatus for testing a semiconductor integrated circuit. The testing apparatus comprises:

-a test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test; and

-a test ancillary device disposed in the vicinity of the test circuit board.

The semiconductor integrated circuit includes an analog-to-digital converter circuit for converting an analog signal to a digital signal or a digital-to-analog converter circuit for converting a digital signal to an analog signal.

The test ancillary device includes data memory for storing digital test data output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal, and an analysis section for analyzing the digital test data stored in the data memory.

The data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose.

The Examiner admits that Toshishige does not disclose a test circuit board, and that the test ancillary device is disposed in the vicinity of the test circuit board.

Also, the Examiner admits that Toshishige does not disclose the claimed structure of the data memory in the test ancillary device.

Rosenthal is relied upon for disclosing the memory divided into two memory sections. However, the Examiner appears to recognize that Rosenthal does not disclose the data memory arranged in the test ancillary device, which is disposed in the vicinity of the test circuit board, as claim 1 requires.

Accordingly, a combination of Toshishige with Rosenthal does not suggest the test ancillary device having the claimed data memory structure, and disposed in the vicinity of the test circuit board, as claim 1 requires.

Yamamura discloses a semiconductor integrated circuit (FIG. 4) including a chip 10a having a core area 12 including circuits 14, which are tested. Also, the chip includes an I/O area 13. "In two corners of the I/O area 13 the test control circuits 15 are placed." (col. 4, lines 6-11). The reference specifies that the test control circuit 15 comprises a decoder and a clock control circuit.

The Examiner considers the test control circuit 15 to correspond to the claimed test ancillary device. Based on a schematic diagram shown in FIG. 4, the Examiner concludes that the test control circuit 15 is "disposed in the vicinity of the chip."

However, as discussed above, the chip contains circuits to be tested. Therefore, one skilled in the art would realize that the chip 10a is not a test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test, as claim 1 requires.

Moreover, Yamamura expressly discloses that the test control circuit 15 does not include the structure of the test ancillary device recited in claim 1.

Accordingly, the previously discussed combination of Toshishige with Rosenthal, combined with Yamamura would not suggest the test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test, and the test ancillary device having the claimed structure and disposed in the vicinity of the test circuit board, as claim 1 requires.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. *Cable Electric Products, Inc. v. Genmark, Inc.*, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated above, the combined teachings of the applied references are not sufficient to arrive at the invention claimed in claim 1. Claims 2-5 dependent from claim 1are defined over the prior art at least for the reasons presented above in connection with claim 1.

Accordingly, the Examiner's rejection of claims 1-5 under 35 U.S.C. 103 is not warranted and should be withdrawn.

Claims 7 and 10-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Rosenthal et al. Claims 8-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige in view of Rosenthal et al. and further in view of Coggins et al.

These rejections are respectfully traversed for the following reasons.

Independent claim 7 recites a method of testing a semiconductor integrated circuit, which includes at least one of an analog-to-digital converter circuit for converting an analog signal to a digital signal and a digital-to-analog converter circuit for converting a digital signal to an analog signal.

The method uses a test circuit board configured to exchange one or more signals with the semiconductor integrated circuit and a test ancillary device coupled to the test circuit board and including a memory having a first and second sections.

The method comprises the step of storing first digital test data derived from the semiconductor integrated circuit in the first memory section while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device configured to analyze digital test data stored in the data memory. The first and second digital test data are one of an output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal.

As discussed above in connection with claim 1, the Examiner admits that Toshishige does not disclose a test circuit board. Accordingly, this reference cannot disclose a test ancillary device coupled to the test circuit board.

Moreover, the Examiner admits that Toshishige does not disclose a test ancillary device including a memory having a first and second sections.

Rosenthal is relied upon for disclosing the memory divided into two memory sections.

However, Rosenthal does not disclose using a test ancillary device coupled to the test circuit board, as claim 7 requires.

Accordingly, a combination of Toshishige with Rosenthal does not teach or suggest a method using a test circuit board configured to exchange one or more signals with the semiconductor integrated circuit and a test ancillary device coupled to the test circuit board and including a memory having a first and second sections.

Moreover, this combination is not sufficient to suggest the step of storing first digital test data derived from the semiconductor integrated circuit in the first memory section of the test ancillary device coupled to the test circuit board, while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device.

Claims 8-12 dependent from claim 7 are defined over the prior art at least for the reasons presented above in connection with claim 7.

Therefore, the rejections of claims 7-12 are not warranted and should be withdrawn.

In view of the foregoing, and in summary, claims 1-5 and 7-12 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension-of-time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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